Abstract of the Disclosure

A central processor unit (CPU) is connected to a system/graphics controller generally comprising a monolithic semiconductor device. The system/graphics controller is connected to an input output (IO) controller via a high-speed PCI bus. The IO controller interfaces to the system graphics controller via the high-speed PCI bus. The IO controller includes a lower speed PCI port controlled by an arbiter within the IO controller. Generally, the low speed PCI arbiter of the IO controller will interface to standard 33 MHz PCI cards. In addition, the IO controller interfaces to an external storage device, such as a hard drive, via either a standard or a proprietary bus protocol. A unified system/graphics memory which is accessed by the system/graphics controller. The unified memory contains both system data and graphics data. In a specific embodiment, two channels, CH0 and CH1 access the unified memory. Each channel is capable of accessing a portion of memory containing graphics data or a portion of memory containing system data. Therefore, it is possible for each channel to access graphics data simultaneously, system data simultaneously, or graphics and system data simultaneously. Simultaneous accesses are facilitated by assuring the physical addresses are partitioned into blocks within the unified memory, such blocks of data are adjacent blocks are accessed by different channels.